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Photonic Advanced Research And Development for Integrated Generic Manufacturing

Welcome to the first newsletter of the EU FP7 PARADIGM project. The objective of PARADIGM is to effect a fundamental change in the way photonic integrated circuits (PICs) based on indium phosphide (InP) are designed and manufactured in Europe. The primary aim is to reduce the costs of design, development and manufacture of PICs by more than an order of magnitude whilst enabling more complex and capable designs possible than ever before.

The key step is to develop a generic platform technology for application-specific PICs. This will be achieved by adopting a similar methodology in the field of photonics to the one that has been so successful in microelectronics. The new approach developed in PARADIGM will be indispensable in creating a sustainable business sector with potential for significant future growth. PARADIGM addresses the whole product development chain from concept, through design and manufacturing to application. It will establish library-based design, coupled with standardized technology process flows and supported by sophisticated design tools. Our goal is to develop technical capability at the platform level, rather than at the level of individual designs, greatly reducing the cost and time required to bring a new component into production, whilst allowing the designer great freedom for creativity at the circuit level.

To establish a generic, design-rule and library-based methodology for photonic ICs is an ambitious and demanding task, which could only be contemplated with a consortium possessing a wide range of complementary skills. PARADIGM has brought together just such a collaboration of Europe's key players in the fields of III-V semiconductor manufacturing, PIC design and applications, photonic CAD, packaging and assembly. The project will verify the potential of the generic approach by fabricating a number of InP PICs, addressing a range of applications in communications, sensors, data processing and biomedical systems, at a level of complexity and performance that will define the state of the art.

In this newsletter we focus on work underway to address the cost-effective packaging of PICs developed within the project, a topic that is vital to the ultimate commercial success of this branch of photonics.



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A PARADIGM Shift for Photonics Packaging

In PARADIGM we are pursuing 3 approaches for PIC packaging which will address the needs of very different chip types. Linkra (www.linkra.it) will use conventional low-cost packaging techniques to demonstrate their use with some of the simpler PIC designs with low connectivity requirements. The Centre for Integrated Photonics (www.ciphotonics.com) will extend their HyBoard™ hybrid packaging platform to enable PICs with high port counts to be used. For the majority of applications caught between these two approaches a third approach is being explored.

The normal procedure for photonics packaging (unlike semiconductor packaging) is to design a bespoke package to suit the chip with minimal attention to using a truly standard package. However the approach being taken in this part of PARADIGM is to reverse this process and design a package capable of standardisation, both in its physical form and functional attributes, and also from a manufacturing standpoint. All of these features should lead to reduced packaging costs and reduced lead-times. Truly a paradigm shift for photonics packaging!

The need for standardisation of critical high volume high performance packaging has been recognised by the IEC, the International Electrotechnical Committee who have standardised the ROSA (receiver optical sub assembly) and TOSA (transmitter optical sub assembly) package formats used in many high speed transceiver products used in high volume for both datacom and telecom applications (Fig 1).



Fig 1 – OCLARO TOSA

These two packages are then combined to sit side by side in the transceiver as shown in Fig 2. For the enhanced functionality offered by PICs it would seem sensible to combine the footprint of the TOSA and ROSA to produce a single larger package (Fig 3) capable of fitting within the standard transceiver package body, such as the XFP.

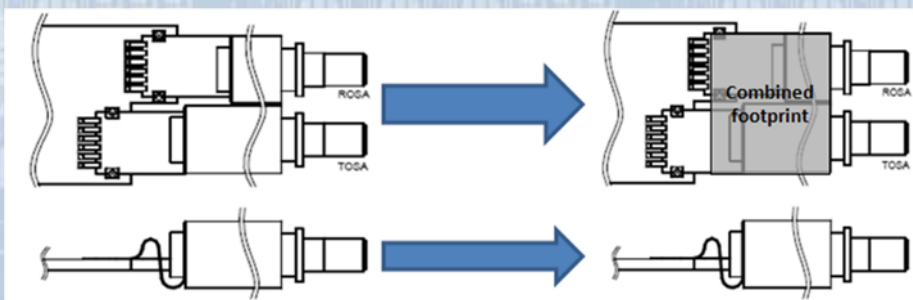


Fig 2 ROSA/TOSA transceiver

Fig 3 Common footprint

A new low port count package (Fig 4) has been designed with the following objectives.

- Standardised package format (potential IEC adoption)
- Captures connectivity requirements for ~80% of envisaged low port count PICs
- XFP and other electronics package compatible
- TEC support
- Flex PCB / leadframe / wirebond interface
- PIC support – POSA (PIC optical sub-assembly)
- Supports single/dual fibre port
- Pigtail and optical connector compatible
- Supports high electrical port count
- Supports high speed

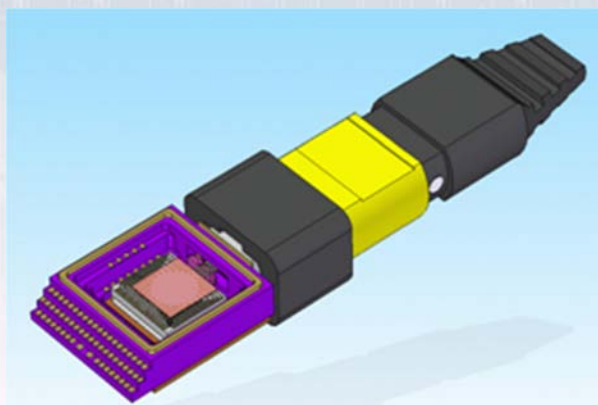


Fig 4 POSA package with PIC and optical connector

This new POSA (PIC Optical Sub Assembly), measuring just 15.5 x 18 x 5mm, with an internal active device cavity ~9.5mm square will support at least 4 x 10Gb/s RF lines along with at least 36 DC connections and a high current TEC connection. The package has been designed in conjunction with one of the largest manufacturers of this style of package to ensure the highest performance, best price and manufacturability. This will ensure compatibility with many high volume ROSA and TOSA manufacturing lines and also with typical prototyping capabilities associated with many foundries. All of these factors should help minimise cycle times for new products with the best cost.

European Photonic Integration Forum, Eindhoven, 21 June '11

The Third European Integration Forum, jointly organised by TU Eindhoven, Oclaro and the University of Ghent, took place recently in Eindhoven. In the morning sessions five speakers discussed application of PICs for long haul and metro networks, access networks, interconnect, fibre sensing and medical applications. In the afternoon an overview of the role of the Photonics21 platform and an introduction on the generic foundry concept was given, after which five presentations were given about the status of generic foundry initiatives in Europe and the US:

- JePPIX, the InP-based platform, including the EuroPIC and PARADIGM projects;
- ePIXfab, the silicon photonics platform, including the HELIOS and WADIMOS projects,
- The dielectric platform TriPleX.
- The US Silicon Photonics platform OPSIS
- US-based hybrid InP platform CHIPfab.

The forum attracted more than 100 attendees and was received very positively. Two-thirds of the audience was from universities, whilst the remainder was from companies and research institutes. Most of the audience came from the Netherlands, but a significant part (30%) from other European countries and 3% from outside Europe (US, Israel). The large attendance and the positive feedback indicate that the photonics community is developing an increased interest in photonic integration in general, and generic integration in particular.

Papers are available here : <http://www.jeppix.eu/documents/37-general/56-epif3.html>

Packaging Workshop

On Thursday 7 July COBRA-TU Eindhoven organised a workshop on packaging, in close cooperation with EuroPIC and PARADIGM partners CIP, Gooch and Housego and Willow Photonics. The Workshop was attended by 26 representatives from a number of key players in the field of photonic packaging: CIP, Gooch and Housego, IZM, TE connectivity (former Tyco Electronics) and Oclaro. Also present were a number of companies and institutes that are interested in using these packages: SATRAX, Universities of Eindhoven, Cambridge and Berlin, 2M Engineering, Technobis and TNO.

In the morning a number of packaging providers presented overviews of their technology and their view on future developments, and in the afternoon a number of users presented their requirements. The day was considered very fruitful by all attendants and significant steps towards a high degree of standardisation were proposed and positively received. Once again it seems that Europe is clearly setting the trend in this area.

Papers are available here : http://www.jeppix.eu/document_store/